DATA SHEET

TDA9852
I²C-bus controlled BTSC stereo/SAP decoder and audio processor

Preliminary specification
Supersedes data of 1996 Feb 28
File under Integrated Circuits, IC02

1997 Mar 11

Philips Semiconductors

PHILIPS

I²C-bus controlled BTSC stereo/SAP decoder and audio processor

TDA9852

FEATURES

- Quasi alignment-free application due to automatic adjustment of channel separation via I²C-bus
- High integration level with automatically tuned integrated filters
- Input level adjustment I²C-bus controlled
- Alignment-free SAP processing
- dbx noise reduction circuit
- Power supply
- I²C-bus transceiver.

Stereo decoder

- Stereo pilot PLL circuit with ceramic resonator, automatic adjustment procedure for stereo channel separation, two pilot thresholds selectable via I²C-bus.

Audio processor

- Selector for internal and external signals (line in)
- Automatic volume level control (control range +6 to −15 dB)
- Interface for external noise reduction circuits
- Volume control (control range +16 to −71 dB)
- Special loudness characteristic automatically controlled in combination with volume setting (control range 28 dB)
- Audio signal zero crossing detection between any volume step switching
- Mute control at audio signal zero crossing
- Mute control via I²C-bus.

GENERAL DESCRIPTION

The TDA9852 is a bipolar-integrated BTSC stereo decoder with hi-fi audio processor (I²C-bus controlled) for application in TV sets, VCRs and multimedia.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9852	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1
TDA9852H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

LICENSE INFORMATION

A license is required for the use of this product. For further information, please contact

COMPANY	BRANCH	ADDRESS
THAT Corporation	Licensing Operations	734 Forest St. Marlborough, MA 01752 USA Tel.: (508) 229-2500 Fax: (508) 229-2590
	Tokyo Office	405 Palm House, 1-20-2 Honmachi Shibuya-ku, Tokyo 151 Japan Tel.: (03) 3378-0915 Fax: (03) 3374-5191

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		8.0	8.5	9.0	V
I_{CC}	supply current		–	75	95	mA
$V_{comp(rms)}$	input signal voltage (RMS value)	100% modulation L + R; f_i = 300 Hz	–	250	–	mV
$V_{oR,L(rms)}$	output signal voltage (RMS value)	100% modulation L + R; f_i = 300 Hz	–	500	–	mV
G_{LA}	input level adjustment control		–3.5	–	+4.0	dB
α_{cs}	stereo channel separation	f_L = 300 Hz; f_R = 3 kHz	25	35	–	dB
$THD_{L,R}$	total harmonic distortion L + R	f_i = 1 kHz	–	0.2	–	%
$V_{I, O(rms)}$	signal handling (RMS value)	THD < 0.5%	2	–	–	V
AVL	control range		–15	–	+6	dB
G_C	volume control range		–71	–	+16	dB
L_B	maximum loudness boost	f_i = 40 Hz	–	17	–	dB
S/N	signal-to-noise ratio	line out (mono); V_o = 0.5 V (RMS)				
		CCIR noise weighting filter (peak value)	–	60	–	dB
		DIN noise weighting filter (RMS value)	–	73	–	dBA
S/N	signal-to-noise ratio	audio section; V_o = 2 V (RMS); gain = 0 dB				
		CCIR noise weighting filter (peak value)	–	94	–	dB
		DIN noise weighting filter (RMS value)	–	107	–	dBA

BLOCK DIAGRAM

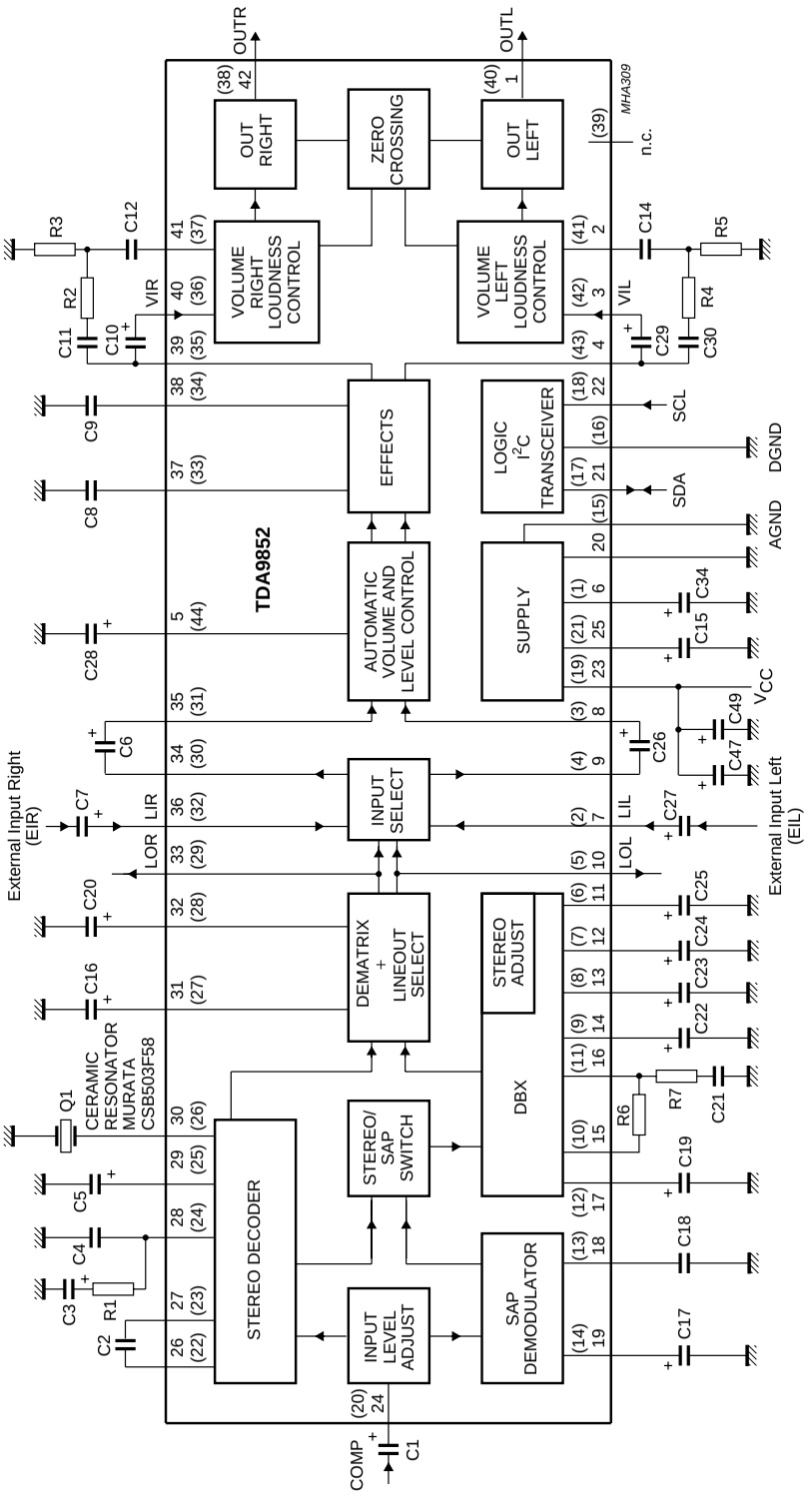


Fig.1 Block diagram.

The numbers given in parenthesis refer to the TDA9852H version.

Component list

Electrolytic capacitors ±20%; foil or ceramic capacitors ±10%; resistors ±5%; unless otherwise specified; see Fig.1.

COMPONENTS	VALUE	TYPE	REMARK
C1	10 µF	electrolytic	63 V
C2	470 nF	foil	
C3	4.7 µF	electrolytic	63 V
C4	220 nF	foil	
C5	10 µF	electrolytic	63 V; I_{leak} < 1.5 µA
C6	2.2 µF	electrolytic	16 V
C7	2.2 µF	electrolytic	63 V
C8	15 nF	foil	±5%
C9	15 nF	foil	±5%
C10	2.2 µF	electrolytic	16 V
C11	8.2 nF	foil or ceramic	±5% SMD 2220/1206
C12	150 nF	foil	±5%
C14	150 nF	foil	±5%
C15	100 µF	electrolytic	16 V
C16	4.7 µF	electrolytic	63 V
C17	4.7 µF	electrolytic	63 V
C18	100 nF	foil	
C19	10 µF	electrolytic	63 V
C20	4.7 µF	electrolytic	63 V
C21	47 nF	foil	±5%
C22	1 µF	electrolytic	63 V
C23	1 µF	electrolytic	63 V
C24	10 µF	electrolytic	63 V ±10%
C25	10 µF	electrolytic	63 V ±10%
C26	2.2 µF	electrolytic	16 V
C27	2.2 µF	electrolytic	63 V
C28	4.7 µF	electrolytic	63 V ±10%
C29	2.2 µF	electrolytic	16 V
C30	8.2 nF	foil or ceramic	±5% SMD 2220/1206
C34	100 µF	electrolytic	16 V
C47	220 µF	electrolytic	25 V
C49	100 nF	foil or ceramic	SMD 1206
R1	2.2 kΩ	–	
R2	20 kΩ	–	
R3	2.2 kΩ	–	
R4	20 kΩ	–	
R5	2.2 kΩ	–	
R6	8.2 kΩ	–	±2%

COMPONENTS	VALUE	TYPE	REMARK
R7	160 Ω	–	±2%
Q1		CSB503F58	radial leads
		CSB503JF958	alternative as SMD

PINNING

SYMBOL	PINS		DESCRIPTION
	SDIP42	QFP44	
OUTL	1	40	output, left channel
LDL	2	41	input loudness, left channel
VIL	3	42	input volume, left channel
EOL	4	43	output effects, left channel
C_{AV}	5	44	automatic volume control capacitor
V_{ref}	6	1	reference voltage $0.5V_{CC}$
LIL	7	2	input line control, left channel
AVL	8	3	input automatic volume control, left channel
SOL	9	4	output selector, left channel
LOL	10	5	output line control, left channel
C_{TW}	11	6	capacitor timing wideband for dbx
C_{TS}	12	7	capacitor timing spectral for dbx
C_W	13	8	capacitor wideband for dbx
C_S	14	9	capacitor spectral for dbx
VEO	15	10	variable emphasis output for dbx
VEI	16	11	variable emphasis input for dbx
C_{NR}	17	12	capacitor noise reduction for dbx
C_M	18	13	capacitor mute for SAP
C_{DEC}	19	14	capacitor DC-decoupling for SAP
GND	20	–	ground
AGND	–	15	analog ground
DGND	–	16	digital ground
SDA	21	17	serial data input/output (I²C-bus)
SCL	22	18	serial clock input (I²C-bus)
V_{CC}	23	19	supply voltage
COMP	24	20	composite input signal
V_{CAP}	25	21	capacitor for electronic filtering of supply
C_{P1}	26	22	capacitor for pilot detector
C_{P2}	27	23	capacitor for pilot detector
C_{PH}	28	24	capacitor for phase detector
C_{ADJ}	29	25	capacitor for filter adjustment
CER	30	26	ceramic resonator
C_{MO}	31	27	capacitor DC-decoupling mono

SYMBOL	PINS		DESCRIPTION
	SDIP42	QFP44	
C_{SS}	32	28	capacitor DC-decoupling stereo/SAP
LOR	33	29	output line control, right channel
SOR	34	30	output selector, right channel
AVR	35	31	input automatic volume control, right channel
LIR	36	32	input line control, right channel
C_{PS2}	37	33	capacitor 2 pseudo function
C_{PS1}	38	34	capacitor 1 pseudo function
EOR	39	35	output effects, right channel
VIR	40	36	input volume, right channel
LDR	41	37	input loudness, right channel
OUTR	42	38	output, right channel
n.c.	–	39	not connected

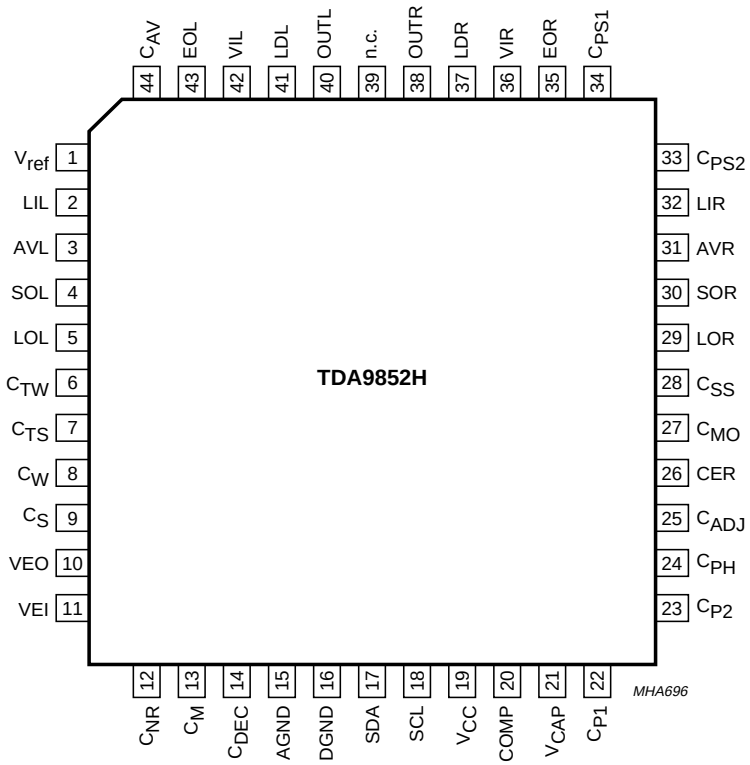


Fig.2 Pin configuration (QFP-version).

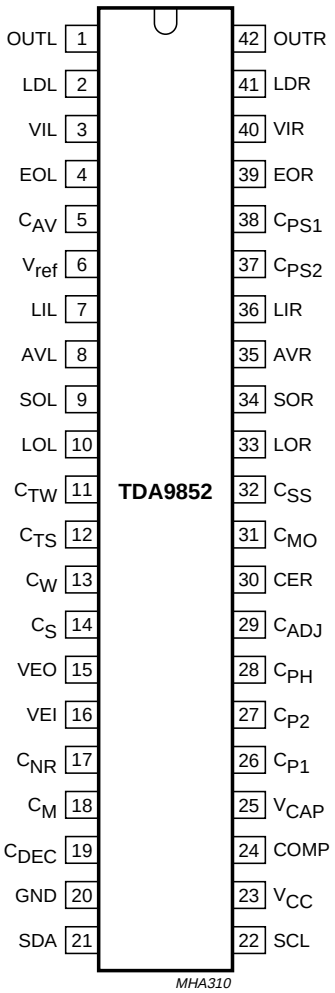


Fig.3 Pin configuration (SDIP-version).

FUNCTIONAL DESCRIPTION

Stereo decoder

INPUT LEVEL ADJUSTMENT

The composite input signal is fed to the input level adjustment stage. The control range is from –3.5 to +4.0 dB in steps of 0.5 dB. The subaddress control 3 of Tables 5 and 6 and the level adjust setting of Table 21 allows an optimum signal adjustment during the set alignment. The maximum input signal voltage is 2 V (RMS).

STEREO DECODER

The output signal of the level adjustment stage is coupled to a low-pass filter which suppresses the baseband noise above 125 kHz. The composite signal is then fed into a pilot detector/pilot cancellation circuit and into the MPX demodulator. The main L + R signal passes a 75 μs fixed de-emphasis filter and is fed into the dematrix circuit.
The decoded sub-signal L – R is sent to the stereo/SAP switch. To generate the pilot signal the stereo demodulator uses a PLL circuit including a ceramic resonator.
The stereo channel separation is adjusted by an automatic procedure to be performed during set production. For a detailed description see Section “Adjustment procedure”.
The stereo identification can be read by the I²C-bus (see Table 2). Two different pilot thresholds (data STS = 1; STS = 0) can be selected via the I²C-bus (see Table 19).

SAP DEMODULATOR

The composite signal is fed from the output of the input level adjustment stage to the SAP demodulator circuit through a $5f_H$ (f_H = horizontal frequency) band-pass filter. The demodulator level is automatically controlled.
The SAP demodulator includes internal noise and field strength detectors that mute the SAP output in the event of insufficient signal conditions. The SAP identification signal can be read by the I²C-bus (see Table 2).

SWITCH

The stereo/SAP switch feeds either the L – R signal or the SAP demodulator output signal via the internal dbx noise reduction circuit to the dematrix/switching circuit. Table 12 shows the different switch modes provided at the output pins LOR and LOL.

dbx DECODER

The circuit includes all blocks required for the noise reduction system in accordance with the BTSC system specification. The output signal is fed through a 73 µs fixed de-emphasis circuit to the dematrix block.

INTEGRATED FILTERS

The filter functions necessary for stereo and SAP demodulation and part of the dbx filter circuits are provided on-chip using transconductor circuits. The required filter accuracy is attained by an automatic filter alignment circuit.

Audio processor

SELECTOR

The selector allows selecting either the internal line out signals LOR or LOL (dematrix output) or the external line in signals LIR and LIL and combines the left and right signals in several modes (see Tables 5 and 6 for subaddress and Table 11 for data). The input signal capability of the line inputs (LIR/LIL) is 2 V (RMS).
The output of the selector is AC-coupled to the automatic volume level control circuit via pins SOR/SOL and AVR/AVL to avoid offset voltages.

AUTOMATIC VOLUME LEVEL CONTROL

The automatic volume level stage controls its output voltage to a constant level of typically 200 mV (RMS) from an input voltage range of 0.1 to 1.1 V (RMS). The circuit adjusts variations in modulation during broadcasting and due to changes in the programme material. The function can be switched **off**. To avoid audible 'plops' during the permanent operation of the AVL circuit a soft blending scheme has been applied between the different gain stages. A capacitor (4.7 µF) at pin C_{AV} determines the attack and decay time constants. In addition the ratio of attack and decay time can be changed via I²C-bus (see Table 15). At power **on**, the discharged 4.7 µF capacitor at C_{AV} must be loaded by the internal decay current. If AVL is chosen, this would result in an attenuated AVL gain for about 10 seconds after power **on**. This can be speeded up by choosing via I²C-bus an increased charge current (about 10 times higher) for about the first 2 seconds after power **on** (see Table 6, CCD bit in control 1 and Table 18).

EFFECTS

The audio processor section offers the following mode selections: linear stereo, pseudo stereo, spatial stereo and forced mono.The spatial mode provides an antiphase crosstalk of 30% or 52% (switchable via I²C-bus; see Table 10).

VOLUME/LOUDNESS

The volume control range is from +16 dB to –71 dB in steps of 1 dB and ends with a mute step (see Table 8). Balance control is achieved by the independent volume control of each channel. The volume control blocks operate in combination with the loudness control. The filter is linear when maximum gain for volume control is selected. The filter characteristic changes automatically over a range of 28 dB down to a setting of –12 dB. At –12 dB volume control the maximum loudness boost is obtained. The filter characteristic is determined by external components. The proposed application provides a maximum boost of 17 dB for bass and 4.5 dB for treble. The loudness may be switched **on** or **off** via I²C-bus control (see Table 9). The left and right volume control stages include two independent zero crossing detectors. A change in volume is automatically activated but not executed. The execution is enabled at the next zero crossing of the signal. If a new volume step is activated before the previous one has been processed, the previous value will be executed first, and then the new value will be activated. If no zero crossing occurs the next volume transmission will enforce the last activated volume setting.

The zero crossing is realized between adjoining steps and between any steps, but not from any step to mute. In this case the GMU bit is needed to use. In case only one channel has to be muted, two steps are necessary. The first step is a transmission of any step to –71 dB and the second step is the –71 dB step to mute mode. The step of –71 dB to mute mode has no zero crossing but this is not relevant.

MUTE

The mute function can be activated independently with last step of volume control at the left or right output. By setting the general mute bit GMU via the I²C-bus all outputs are muted. All channels include an independent zero cross detector. The zero crossing mute feature can be selected via bit TZCM:

TZCM = 0: forced mute with direct execution

TZCM = 1: execution in time with signal zero crossing.

In the zero cross mode a change in the GMU polarity is activated but not executed. The execution is enabled at the next zero crossing of the signal. To avoid a large delay of mute switching, when very low frequencies are processed, or the output signal amplitude is lower than the DC offset voltage, the following I²C-bus transmissions are needed:

a first transmission for mute execution

a second transmission about 100 ms later, which must switch the zero crossing mode to forced mute (TZCM = 0)

a third transmission to reactivate the zero crossing mode (TZCM = 1). This transmission can take place immediately, but must follow before the next mute execution.

Adjustment procedure

COMPOSITE INPUT LEVEL ADJUSTMENT

Feed in from FM demodulator the composite signal with 100% modulation (25 kHz deviation) L + R; f_i = 300 Hz. Set input level control via I²C-bus monitoring line out (500 mV ±20 mV). Store the setting in a non-volatile memory.

AUTOMATIC ADJUSTMENT PROCEDURE

- Capacitors of external inputs LIL and LIR must be grounded at EIL and EIR
- Composite input signal L = 300 Hz, R = 3.1 kHz, 14% modulation for each channel; volume gain +16 dB via I²C-bus
- Effects, AVL, loudness **off**.
- Line out setting bits: STEREO = 1, SAP = 0 (see Table 12)
- Selector setting SC0, SC1, SC2 = 0, 0, 0 (see Table 11)
- Start adjustment by transmission ADJ = 1 in register ALI3; the decoder will align itself
- After 1 second minimum stop alignment by transmitting ADJ = 0 in register ALI3 read the alignment data by an I²C-bus read operation from ALR1 and ALR2 (see Chapter “I²C-bus protocol”) and store it in a non-volatile memory; the alignment procedure overwrites the previous data stored in ALI1 and ALI2
- Disconnect the capacitors of external inputs from ground.

MANUAL ADJUSTMENT

Manual adjustment is necessary when no dual tone generator is available (e.g. for service).

- Spectral and wideband data have to be set to 10000 (middle position for adjustment range)
- Composite input L = 300 Hz; 14% modulation
- Adjust channel separation by varying wideband data
- Composite input L = 3 kHz; 14% modulation
- Adjust channel separation by varying spectral data
- Iterative spectral/wideband operation for optimum adjustment
- Store data in non-volatile memory.

TIMING CURRENT FOR RELEASE RATE

Due to possible internal and external spreading, the timing current can be adjusted via I²C-bus, see Table 20, as recommended by dbx.

Requirements for the composite input signal to ensure correct system performance

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$COMP_{L+R(rms)}$	composite input level for 100% modulation L + R; 25 kHz deviation; f_i = 300 Hz; RMS value	measured at COMP	162	250	363	mV
ΔCOMP	composite input level spreading under operating conditions	T_{amb} = –20 to +70 °C; aging; power supply influence	–0.5	–	+0.5	dB
Z_o	output impedance	note 1	–	low-ohmic	5	kΩ
f_{lf}	low frequency roll-off	25 kHz deviation L + R; –2 dB	–	–	5	Hz
f_{hf}	high frequency roll-off	25 kHz deviation L + R; –2 dB	100	–	–	kHz
$THD_{L,R}$	total harmonic distortion L + R	f_i = 1 kHz; 25 kHz deviation	–	–	0.5	%
		f_i = 1 kHz; 125 kHz deviation; note 2	–	–	1.5	%
S/N	signal-to-noise ratio L + R/noise	CCIR 468-2 weighted quasi peak; L + R; 25 kHz deviation; f_i = 1 kHz; 75 μs de-emphasis				
		critical picture modulation; note 3	44	–	–	dB
		with sync only	54	–	–	dB
α_{SB}	side band suppression mono into unmodulated SAP carrier; SAP carrier/side band	mono signal: 25 kHz deviation, f_i = 1 kHz; side band: SAP carrier frequency ±1 kHz	46	–	–	dB
α_{SP}	spectral spurious attenuation L + R/spurious	50 Hz to 100 kHz; mainly n × f_H; no de-emphasis; L + R; 25 kHz deviation, f = 1 kHz as reference				
		n = 1, 5	35	–	–	dB
		n = 4, 6	40	–	–	dB
		n = 2, 3	26	–	–	dB

Notes

1. Low-ohmic preferred, otherwise the signal loss and spreading at COMP, caused by Z_o and the composite input impedance (see Chapter “Characteristics”, Section “Input level adjustment control”) must be taken into account.
2. In order to prevent clipping at over-modulation (maximum deviation in the BTSC system for 100% modulation is 73 kHz).
3. For example colour bar or flat field white; 100% video modulation.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	0	9.5	V
V_n	voltage of all other pins to pin V_{CC}	0	V_{CC}	V
T_{amb}	operating ambient temperature	–20	+70	°C
T_{stg}	storage temperature	–65	+150	°C
V_{es}	electrostatic handling; note 1			

Note

1. Human body model: C = 100 pF; R = 1.5 kΩ; V = 2 kV; Charge device model: C = 200 pF; R = 0 Ω; V = 300 V.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT270-1	43	K/W
	SOT307-2	60	K/W

CHARACTERISTICS

All voltages are measured relative to GND; V_{CC} = 8.5 V; R_s = 600 Ω; R_L = 10 kΩ; C_L = 2.5 nF; AC-coupled; f_i = 1 kHz; T_{amb} = 25 °C; gain control G_v = 0 dB; balance in mid position; loudness **off**; see Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
V_{CC}	supply voltage		8.0	8.5	9.0	V
I_{CC}	supply current		–	75	95	mA
V_{ref}	internal reference voltage at pin V_{ref}		–	4.25	–	V
Input level adjustment control						
G_{LA}	input level adjustment control		–3.5	–	+4.0	dB
G_{step}	step resolution		–	0.5	–	dB
$V_{i(rms)}$	maximum input voltage level (RMS value)		2	–	–	V
Z_i	input impedance		29.5	35	40.5	kΩ
Stereo decoder						
$MPX_{L+R(rms)}$	input voltage level for 100% modulation L + R; 25 kHz deviation (RMS value)	input level adjusted via I²C-bus (L + R; f_i = 300 Hz); monitoring LINE OUT	–	250	–	mV
MPX_{L-R}	input voltage level for 100% modulation L – R; 50 kHz deviation (peak value)		–	707	–	mV
$MPX_{(max)}$	maximum headroom for L + R, L, R	f_{mod} < 15 kHz; THD < 15%	9	–	–	dB
$MPX_{pilot(rms)}$	nominal stereo pilot voltage level (RMS value)		–	50	–	mV
$ST_{on(rms)}$	pilot threshold voltage stereo **on** (RMS value)	data STS = 1	–	–	35	mV
		data STS = 0	–	–	30	mV
$ST_{off(rms)}$	pilot threshold voltage stereo **off** (RMS value)	data STS = 1	15	–	–	mV
		data STS = 0	10	–	–	mV
Hys	hysteresis		–	2.5	–	dB
OUT_{L+R}	output voltage level for 100% modulation L + R at LINE OUT	input level adjusted via I²C-bus (L + R; f_i = 300 Hz); monitoring LINE OUT	480	500	520	mV
α_{cs}	stereo channel separation L/R at LINE OUT	aligned with dual tone 14% modulation for each channel; see Section “Adjustment procedure” in Chapter “Functional description”				
		f_L = 300 Hz; f_R = 3 kHz	25	35	–	dB
		f_L = 300 Hz; f_R = 8 kHz	20	30	–	dB
		f_L = 300 Hz; f_R = 10 kHz	15	25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$f_{L,\,R}$	L, R frequency response	14% modulation; f_{ref} = 300 Hz L or R				
		f_i = 50 Hz to 10 kHz	–3	–	–	dB
		f_i = 12 kHz	–	–3	–	dB
$THD_{L,R}$	total harmonic distortion L, R at LINE OUT	modulation L or R 1% to 100%; f_i = 1 kHz	–	0.2	1.0	%
S/N	signal-to-noise ratio	mono mode; CCIR 468-2 weighted; quasi peak; 500 mV output signal	50	60	–	dB
Stereo decoder, oscillator (VCXO); note 1						
f_o	nominal VCXO output frequency ($32f_H$)	with nominal ceramic resonator	–	503.5	–	kHz
f_{of}	spread of free-running frequency	with nominal ceramic resonator	500.0	–	507.0	kHz
Δf_H	capture range frequency (nominal pilot)		±190	±265	–	Hz
SAP demodulator; note 2						
$SAP_{i(rms)}$	nominal SAP carrier input voltage level (RMS value)	15 kHz frequency deviation of intercarrier	–	150	–	mV
$SAP_{on(rms)}$	threshold voltage SAP **on** (RMS value)		–	–	85	mV
$SAP_{off(rms)}$	threshold voltage SAP **off** (RMS value)		35	–	–	mV
SAP_{hys}	hysteresis		–	2	–	dB
SAP_{LEV}	SAP output voltage level at LINE OUT	mode selector in position SAP/SAP; f_{mod} = 300 Hz; 100% modulation	–	500	–	mV
f_{res}	frequency response	14% modulation; 50 Hz to 8 kHz; f_{ref} = 300 Hz	–3	–	–	dB
THD	total harmonic distortion	f_i = 1 kHz	–	0.5	2.0	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LINE OUT at pins LOL and LOR						
$V_{o(rms)}$	nominal output voltage (RMS value)	100% modulation	–	500	–	mV
$HEAD_o$	output headroom		9	–	–	dB
Z_o	output impedance		–	80	120	Ω
V_O	DC output voltage		$0.45V_{CC}$	$0.5V_{CC}$	$0.55V_{CC}$	V
R_L	output load resistance		5	–	–	kΩ
C_L	output load capacitance		–	–	2.5	nF
α_{ct}	crosstalk L, R into SAP	100% modulation; f_i = 1 kHz; L or R; mode selector switched to SAP/SAP	50	75	–	dB
	crosstalk SAP into L, R	100% modulation; f_i = 1 kHz; SAP; mode selector switched to stereo	50	70	–	dB
ΔV_{ST-SAP}	output voltage difference if switched from L, R to SAP	250 Hz to 6.3 kHz	–	–	3	dB
dbx noise reduction circuit						
t_{adj}	stereo adjustment time	see Section “Adjustment procedure” in Chapter “Functional description”	–	–	1	s
I_s	nominal timing current for nominal release rate of spectral RMS detector	I_s can be measured at pin C_{TS} via current meter connected to $\frac{1}{2}V_{CC}$ + 1 V	–	24	–	µA
ΔI_S	spread of timing current		–15	–	+15	%
$I_{s\ range}$	timing current range	7 steps via I²C-bus	–	±30	–	%
I_t	timing current for release rate of wideband RMS detector		–	$\frac{1}{3}I_s$	–	µA
Rel_{rate}	nominal RMS detector release rate	nominal timing current and external capacitor values				
		wideband	–	125	–	dB/s
		spectral	–	381	–	dB/s

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Circuit section from pins LIL and LIR to pins OUTL and OUTR; note 3						
B	roll-off frequencies	C_6, C_7, C_{10}, C_{26}, C_{27} and C_{29} = 2.2 µF; $Z_i = Z_{i(min)}$				
		low frequency (–3 dB)	–	–	20	Hz
		high frequency (–0.5 dB)	20	–	–	kHz
THD	total harmonic distortion	V_i = 1000 mV; G_v = 0 dB; AVL **on**	–	0.2	0.5	%
		V_i = 2000 mV; G_v = 0 dB; AVL **on**	–	0.2	0.5	%
		V_i = 1000 mV; G_v = 0 dB; AVL **off**	–	0.02	–	%
		V_i = 2000 mV; G_v = 0 dB; AVL **off**	–	0.02	–	%
RR	ripple rejection	$V_{r(rms)}$ < 200 mV; f_i = 100 Hz	47	50	–	dB
α_{ct}	crosstalk between bus inputs and signal outputs	notes 4 and 5	–	110	–	dB
V_{no}	noise output voltage	CCIR 468-2 weighted; quasi peak; AVL **off**; loudness **off**; G_v = 0 dB	–	40	80	µV
		measured in dBA; AVL **off**; loudness **off**; G_v = 0 dB	–	8	–	µV
α_{cs}	channel separation	V_i = 1 V; f_i = 1 kHz	75	–	–	dB
		V_i = 1 V; f_i = 12.5 kHz	75	–	–	dB
Effect controls						
α_{spat1}	anti-phase crosstalk by spatial effect		–	52	–	%
α_{spat2}			–	30	–	%
φ	phase shift by pseudo-stereo	see Fig.4	–	–	–	–

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic volume level control (AVL)						
Z_i	input impedance		8.8	11.0	13.2	kΩ
$V_{i(rms)}$	maximum input voltage (RMS value)	THD < 0.2%	2	tbf	–	V
G_v	gain, maximum boost		5	6	7	dB
	maximum attenuation		14	15	16	dB
G_{step}	equivalent step width between the input stages (soft switching system)		–	1.5	–	dB
$V_{iop(rms)}$	input level at maximum boost (RMS value)		–	0.1	–	V
	input level at maximum attenuation (RMS value)		–	1.125	–	V
$V_{o(rms)}$	output level in AVL operation (RMS value)	see Fig.5	160	200	250	mV
$V_{DC\ OFF}$	DC offset between different gain steps	voltage at pin C_{AV} 6.50 to 6.33 V or 6.33 to 6.11 V or 6.11 to 5.33 V or 5.33 to 2.60 V; note 6	–	–	6	mV
R_{att}	discharge resistors for attack time constant	AT1 = 0; AT2 = 0; note 7	340	420	520	Ω
		AT1 = 1; AT2 = 0; note 7	590	730	910	Ω
		AT1 = 0; AT2 = 1; note 7	0.96	1.2	1.5	kΩ
		AT1 = 1; AT2 = 1; note 7	1.7	2.1	2.6	kΩ
I_{dec}	charge current for decay time	normal mode; CCD = 0; note 8	1.6	2.0	2.4	μA
		power-**on** speed-up; CCD = 1; note 8	–	tbf	–	μA
Selector from pins LOL, LOR, LIL and LIR to pins SOL and SOR						
Z_i	input impedance		16	20	24	kΩ
α_s	input isolation of one selected source to the other input	V_i = 1 V; f_i = 1 kHz	86	96	–	dB
		V_i = 1 V; f_i = 12.5 kHz	80	96	–	dB
$V_{i(rms)}$	maximum input voltage (RMS value)	THD < 0.5%	2	2.3	–	V
$V_{DC\ OFF}$	DC offset voltage at selector output by selection of any inputs		–	–	25	mV
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		5	–	–	kΩ
C_L	output load capacitance		0	–	2.5	nF
G_v	voltage gain, selector		–	0	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio control part; input pins VIL and VIR to pins OUTX and OUTS						
Z_i	volume input impedance		8.0	10.0	12.0	kΩ
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		5	–	–	kΩ
C_L	output load capacitance		0	–	2.5	nF
$V_{i(rms)}$	maximum input voltage (RMS value)	THD < 0.5%	2.0	2.15	–	V
V_{no}	noise output voltage	CCIR 468-2 weighted; quasi peak				
		G_v = 16 dB	–	110	220	μV
		G_v = 0 dB	–	33	50	μV
		mute position	–	10	–	μV
G_c	total continuous control range	maximum boost	–	16	–	dB
		maximum attenuation	–	71	–	dB
G_{step}	step resolution		–	1	–	dB
	step error between adjoining step		–	–	0.5	dB
ΔG_a	attenuator set error	G_v = +16 to –50 dB	–	–	2	dB
		G_v = –51 to –71 dB	–	–	3	dB
ΔG_L	gain tracking error	G_v = +16 to –50 dB	–	–	2	dB
α_m	mute attenuation		80	–	–	dB
$V_{DC\ OFF}$	DC step offset between any adjacent step	G_v = +16 to 0 dB	–	0.2	10.0	mV
		G_v = 0 to –71 dB	–	–	5	mV
	DC step offset between any step to mute	G_v = +16 to +1 dB	–	2	15	mV
		G_v = 0 to –71 dB	–	1	10	mV
Loudness control part						
L_B	maximum loudness boost	loudness **on**; referred to loudness **off**; boost is determined by external components; see Fig.6				
		f_i = 40 Hz	–	17	–	dB
		f_i = 10 kHz	–	4.5	–	dB
L_G	loudness control range		–12	–	+16	
Muting at power supply drop for OUTR and OUTS						
$V_{CC\text{-}DROP}$	supply drop for mute active		–	V_{CAP} – 0.7	–	V
Power-on reset; note 9						
$V_{RESET(STA)}$	start of reset voltage	increasing supply voltage	–	–	2.5	V
		decreasing supply voltage	4.2	5	5.8	V
$V_{RESET(END)}$	end of reset voltage	increasing supply voltage	5.2	6	6.8	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital part (I²C-bus pins); note 10						
V_{IH}	HIGH level input voltage		3	–	V_{CC}	V
V_{IL}	LOW level input voltage		–0.3	–	+1.5	V
I_{IH}	HIGH level input current		–10	–	+10	µA
I_{IL}	LOW level input current		–10	–	+10	µA
V_{OL}	LOW level output voltage	I_{IL} = 3 mA	–	–	+0.4	V

Notes to the characteristics

1. The oscillator is designed to operate together with MURATA resonator CSB503F58. Change of the resonator supplier is possible, but the resonator specification must be close to CSB503F58.
2. The internal SAP carrier level is determined by the composite input level and the level adjustment gain.
3. Frequency range 20 Hz to 20 kHz; select in to input line control; effects: linear stereo.
4. Crosstalk: $20 \log \frac{V_{bus(p-p)}}{V_{o(rms)}}$
5. The transmission contains:
   a) Total initialization with MAD and SAD for volume and 11 DATA words, see also definition of characteristics
   b) Clock frequency = 50 kHz
   c) Repetition burst rate = 400 Hz
   d) Maximum bus signal amplitude = 5 V (p-p).
6. The listed pin voltage corresponds with typical gain steps of +6 dB, +3 dB, 0 dB, –6 dB and –15 dB.
7. Attack time constant = $C_{AV} \times R_{att}$.
8. Decay time $= \frac{C_{AV} \times 0.76\ V \left(10^{\frac{-G_1}{20}} - 10^{\frac{-G_2}{20}} \right)}{I_{dec}}$

   Example: C_{AV} = 4.7 µF; I_{dec} = 2 µA; G_1 = –9 dB; G_2 = +6 dB → decay time results in 4.14 s.
9. When reset is active the GMU-bit (general mute) and the LMU-bit (LINE OUT mute) is set and the I²C-bus receiver is in the reset position.
10. The AC characteristics are in accordance with the I²C-bus specification. The maximum clock frequency is 100 kHz. Information about the I²C-bus can be found in the brochure *"The I²C-bus and how to use it"* (order number 9398 393 40011).

I²C-BUS PROTOCOL

I²C-bus format to read (slave transmits data)

S	SLAVE ADDRESS	R/$\overline{W}$	A	DATA	MA	DATA	P

Table 1 Explanation of I²C-bus format to read (slave transmits data)

NAME	DESCRIPTION
S	START condition; generated by the master
Standard SLAVE ADDRESS (MAD)	101 101 1
R/$\overline{W}$	1 (read); generated by the master
A	acknowledge; generated by the slave
DATA	slave transmits an 8-bit data word
MA	acknowledge; generated by the master
P	STOP condition; generated by the master

Table 2 Definition of the transmitted bytes after read condition

FUNCTION	BYTE	MSB							LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Alignment read 1	ALR1	Y	SAPP	STP	A14	A13	A12	A11	A10
Alignment read 2	ALR2	Y	SAPP	STP	A24	A23	A22	A21	A20

Table 3 Function of the bits in Table 2

BITS	FUNCTION
STP	stereo pilot identification (stereo received = 1)
SAPP	SAP pilot identification (SAP received = 1)
A1X to A2X	stereo alignment read data
A1X	for wideband expander
A2X	for spectral expander
Y	indefinite

The master generates an acknowledge when it has received the first data word ALR1, then the slave transmits the next data word ALR2. Afterwards the master generates an acknowledge, then the slave begins transmitting the first data word ALR1 etc. until the master generates no acknowledge and transmits a STOP condition.

I²C-bus format to write (slave receives data)

S	SLAVE ADDRESS	R/$\overline{W}$	A	SUBADDRESS	A	DATA	A	P

Table 4 Explanation of I²C-bus format to write (slave receives data)

NAME	DESCRIPTION
S	START condition
Standard SLAVE ADDRESS (MAD)	101 101 1
R/$\overline{W}$	0 (write)
A	acknowledge; generated by the slave
SUBADDRESS (SAD)	see Table 5
DATA	see Table 6
P	STOP condition

If more than 1 byte of DATA is transmitted, then auto-increment is performed, starting from the transmitted subaddress and auto-increment of subaddress in accordance with the order of Table 5 is performed.

Table 5 Subaddress second byte after MAD

FUNCTION	REGISTER	MSB							LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Volume right	VR	0	0	0	0	0	0	0	0
Volume left	VL	0	0	0	0	0	0	0	1
Control 1 (note 1)	CON1	0	0	0	0	0	1	0	1
Control 2	CON2	0	0	0	0	0	1	1	0
Control 3	CON3	0	0	0	0	0	1	1	1
Alignment 1	ALI1	0	0	0	0	1	0	0	0
Alignment 2	ALI2	0	0	0	0	1	0	0	1
Alignment 3	ALI3	0	0	0	0	1	0	1	0

Note

1. In auto-increment mode it is necessary to insert 3 dummy data words between volume left and control 1.

Table 6 Definition of third byte, third byte after MAD and SAD

FUNCTION	REGISTER	MSB							LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Volume right	VR	0	VR6	VR5	VR4	VR3	VR2	VR1	VR0
Volume left	VL	0	VL6	VL5	VL4	VL3	VL2	VL1	VL0
Control 1	CON1	GMU	AVLON	LOFF	CCD	0	SC2	SC1	SC0
Control 2	CON2	SAP	STEREO	TZCM	1	LMU	EF2	EF1	EF0
Control 3	CON3	0	0	0	0	L3	L2	L1	L0
Alignment 1	ALI1	0	0	0	A14	A13	A12	A11	A10
Alignment 2	ALI2	STS	0	0	A24	A23	A22	A21	A20
Alignment 3	ALI3	ADJ	AT1	AT2	0	1	TC2	TC1	TC0

Table 7 Function of the bits in Table 6

BITS	FUNCTION
VR0 to VR6	volume control right
VL0 to VL6	volume control left
GMU	mute control for all outputs (generate mute)
AVLON	AVL **on**/**off**
CCD	increased AVL decay current **on**/**off**
LOFF	switch loudness **on**/**off**
SC0 to SC2	selection between line in and line out
STEREO, SAP	mode selection for line out
TZCM	zero cross mode in mute operation (right and left output stage)
LMU	mute control for line out
EF0 to EF2	selection between mono, stereo linear, spatial stereo and pseudo mode
L0 to L3	input level adjustment
ADJ	stereo adjustment **on**/**off**
A1X to A2X	stereo alignment data
A1X	for wideband expander
A2X	for spectral expander
AT1 and AT2	attack time at AVL
TC0 to TC2	timing current alignment data
STS	stereo level switch

Table 8 Volume setting

FUNCTION G_v (dB)	DATA						
	V6	V5	V4	V3	V2	V1	V0
16	1	1	1	1	1	1	1
15	1	1	1	1	1	1	0
14	1	1	1	1	1	0	1
13	1	1	1	1	1	0	0
12	1	1	1	1	0	1	1
11	1	1	1	1	0	1	0
10	1	1	1	1	0	0	1
9	1	1	1	1	0	0	0
8	1	1	1	0	1	1	1
7	1	1	1	0	1	1	0
6	1	1	1	0	1	0	1
5	1	1	1	0	1	0	0
4	1	1	1	0	0	1	1
3	1	1	1	0	0	1	0
2	1	1	1	0	0	0	1
1	1	1	1	0	0	0	0

FUNCTION G_v (dB)	DATA						
	V6	V5	V4	V3	V2	V1	V0
0	1	1	0	1	1	1	1
–1	1	1	0	1	1	1	0
–2	1	1	0	1	1	0	1
–3	1	1	0	1	1	0	0
–4	1	1	0	1	0	1	1
–5	1	1	0	1	0	1	0
–6	1	1	0	1	0	0	1
–7	1	1	0	1	0	0	0
–8	1	1	0	0	1	1	1
–9	1	1	0	0	1	1	0
–10	1	1	0	0	1	0	1
–11	1	1	0	0	1	0	0
–12	1	1	0	0	0	1	1
–13	1	1	0	0	0	1	0
–14	1	1	0	0	0	0	1
–15	1	1	0	0	0	0	0
–16	1	0	1	1	1	1	1
–17	1	0	1	1	1	1	0
–18	1	0	1	1	1	0	1
–19	1	0	1	1	1	0	0
–20	1	0	1	1	0	1	1
–21	1	0	1	1	0	1	0
–22	1	0	1	1	0	0	1
–23	1	0	1	1	0	0	0
–24	1	0	1	0	1	1	1
–25	1	0	1	0	1	1	0
–26	1	0	1	0	1	0	1
–27	1	0	1	0	1	0	0
–28	1	0	1	0	0	1	1
–29	1	0	1	0	0	1	0
–30	1	0	1	0	0	0	1
–31	1	0	1	0	0	0	0
–32	1	0	0	1	1	1	1
–33	1	0	0	1	1	1	0
–34	1	0	0	1	1	0	1
–35	1	0	0	1	1	0	0
–36	1	0	0	1	0	1	1
–37	1	0	0	1	0	1	0
–38	1	0	0	1	0	0	1

FUNCTION G_v (dB)	DATA						
	V6	V5	V4	V3	V2	V1	V0
−39	1	0	0	1	0	0	0
−40	1	0	0	0	1	1	1
−41	1	0	0	0	1	1	0
−42	1	0	0	0	1	0	1
−43	1	0	0	0	1	0	0
−44	1	0	0	0	0	1	1
−45	1	0	0	0	0	1	0
−46	1	0	0	0	0	0	1
−47	1	0	0	0	0	0	0
−48	0	1	1	1	1	1	1
−49	0	1	1	1	1	1	0
−50	0	1	1	1	1	0	1
−51	0	1	1	1	1	0	0
−52	0	1	1	1	0	1	1
−53	0	1	1	1	0	1	0
−54	0	1	1	1	0	0	1
−55	0	1	1	1	0	0	0
−56	0	1	1	0	1	1	1
−57	0	1	1	0	1	1	0
−58	0	1	1	0	1	0	1
−59	0	1	1	0	1	0	0
−60	0	1	1	0	0	1	1
−61	0	1	1	0	0	1	0
−62	0	1	1	0	0	0	1
−63	0	1	1	0	0	0	0
−64	0	1	0	1	1	1	1
−65	0	1	0	1	1	1	0
−66	0	1	0	1	1	0	1
−67	0	1	0	1	1	0	0
−68	0	1	0	1	0	1	1
−69	0	1	0	1	0	1	0
−70	0	1	0	1	0	0	1
−71	0	1	0	1	0	0	0
Mute	0	1	0	0	1	1	1

Table 9 Loudness setting

CHARACTERISTIC	DATA LOFF
With loudness	0
Linear	1

Table 10 Effects setting

FUNCTION	DATA		
	EF2	EF1	EF0
Stereo linear **on**	0	0	0
Pseudo **on**	0	0	1
Spatial stereo; 30% anti-phase crosstalk	0	1	0
Spatial stereo; 50% anti-phase crosstalk	0	1	1
Forced mono	1	1	1

Table 11 Selector setting

FUNCTION(1)	DATA		
	SC2	SC1	SC0
Inputs LOR and LOL	0	0	0
Inputs LOR and LOR	0	0	1
Inputs LOL and LOL	0	1	0
Inputs LOL and LOR	0	1	1
Inputs LIR and LIL	1	0	0
Inputs LIR and LIR	1	0	1
Inputs LIL and LIL	1	1	0
Inputs LIL and LIR	1	1	1

Note

1. Input connected to outputs SOR and SOL.

Table 12 Switch setting at line out

LINE OUT SIGNALS AT		DATA TRANSMISSION STATUS INTERNAL SWITCH, READABLE BITS: STP, SAPP	SETTING BITS	
LOL	LOR		STEREO	SAP
SAP	SAP	SAP received	1	1
Mute	mute	no SAP received	1	1
Left	right	STEREO received	1	0
Mono	mono	no STEREO received	1	0
Mono	SAP	SAP received	0	1
Mono	mute	no SAP received	0	1
Mono	mono	independent	0	0

Table 13 Zero cross detection setting

FUNCTION	DATA TZCM
Direct mute control	0
Mute control delayed until the next zero crossing	1

Table 14 Mute setting

FUNCTION	DATA GMU	FUNCTION	DATA LMU
Forced mute at OUTR, OUTL and OUTS	1	forced mute at LOR and LOL	1
Audio processor controlled outputs	0	stereo processor controlled outputs	0

Table 15 AVL attack time

FUNCTION	DATA	
	AT1	AT2
R_{att} = 420 Ω	0	0
R_{att} = 730 Ω	1	0
R_{att} = 1200 Ω	0	1
R_{att} = 2100 Ω	1	1

Table 16 ADJ bit setting

FUNCTION	DATA
Stereo decoder operation mode	0
Auto adjustment of channel separation	1

Table 17 AVLON bit setting

FUNCTION	DATA
Automatic volume control **off**	0
Automatic volume control **on**	1

Table 18 CCD bit setting

FUNCTION	DATA
Load current for normal AVL decay time	0
Increased load current	1

Table 19 STS bit setting (pilot threshold stereo **on**)

FUNCTION	DATA
$ST_{on} \leq 35$ mV	1
$ST_{on} \leq 30$ mV	0

Table 20 Timing current setting

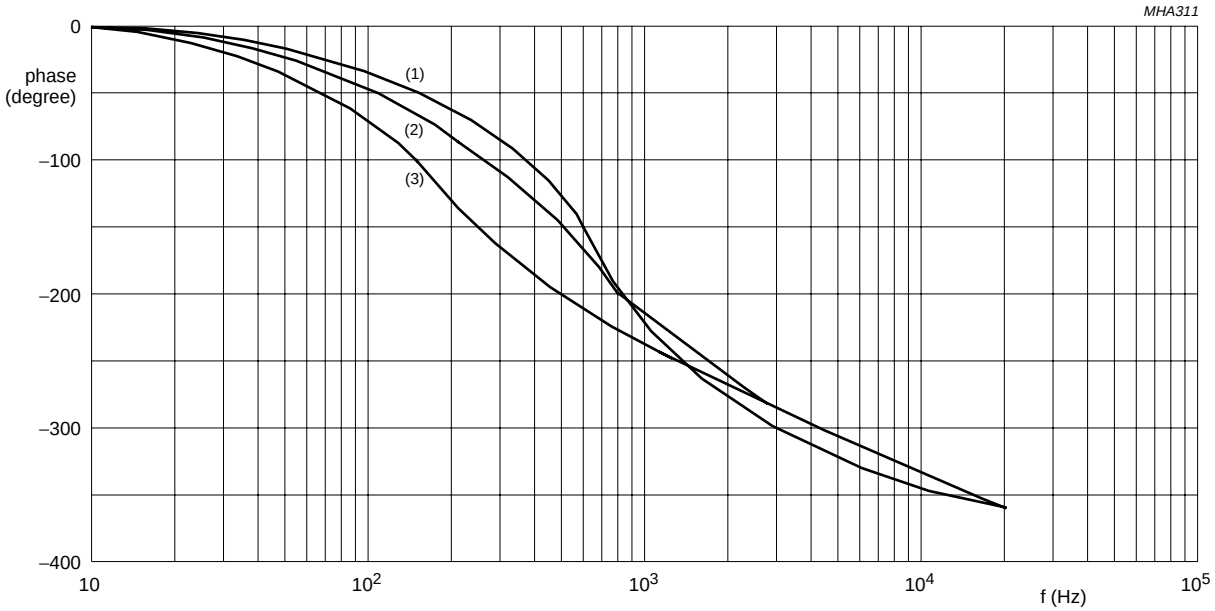
FUNCTION I_S RANGE	DATA		
	TC2	TC1	TC0
+30%	1	0	0
+20%	1	0	1
+10%	1	1	0
Nominal	0	1	1
–10%	0	1	0
–20%	0	0	1
–30%	0	0	0

Table 21 Level adjust setting

G_L (dB)	DATA			
	L3	L2	L1	L0
+4.0	1	1	1	1
+3.5	1	1	1	0
+3.0	1	1	0	1
+2.5	1	1	0	0
+2.0	1	0	1	1
+1.5	1	0	1	0
+1.0	1	0	0	1
+0.5	1	0	0	0
0.0	0	1	1	1
–0.5	0	1	1	0
–1.0	0	1	0	1
–1.5	0	1	0	0
–2.0	0	0	1	1
–2.5	0	0	1	0
–3.0	0	0	0	1
–3.5	0	0	0	0

Table 22 Alignment data for expander in read register ALR1 and ALR2 and in write register ALI1 and ALI2

FUNCTION	DATA				
	D4 AX4	**D3 AX3**	**D2 AX2**	**D1 AX1**	**D0 AX0**
Gain increase	1	1	1	1	1
	1	1	1	1	0
	1	1	1	0	1
	1	1	1	0	0
	1	1	0	1	1
	1	1	0	1	0
	1	1	0	0	1
	1	1	0	0	0
	1	0	1	1	1
	1	0	1	1	0
	1	0	1	0	1
	1	0	1	0	0
	1	0	0	1	1
	1	0	0	1	0
	1	0	0	0	1
Nominal gain	1	0	0	0	0
	0	1	1	1	1
Gain decrease	0	1	1	1	0
	0	1	1	0	1
	0	1	1	0	0
	0	1	0	1	1
	0	1	0	1	0
	0	1	0	0	1
	0	1	0	0	0
	0	0	1	1	1
	0	0	1	1	0
	0	0	1	0	1
	0	0	1	0	0
	0	0	0	1	1
	0	0	0	1	0
	0	0	0	0	1
	0	0	0	0	0

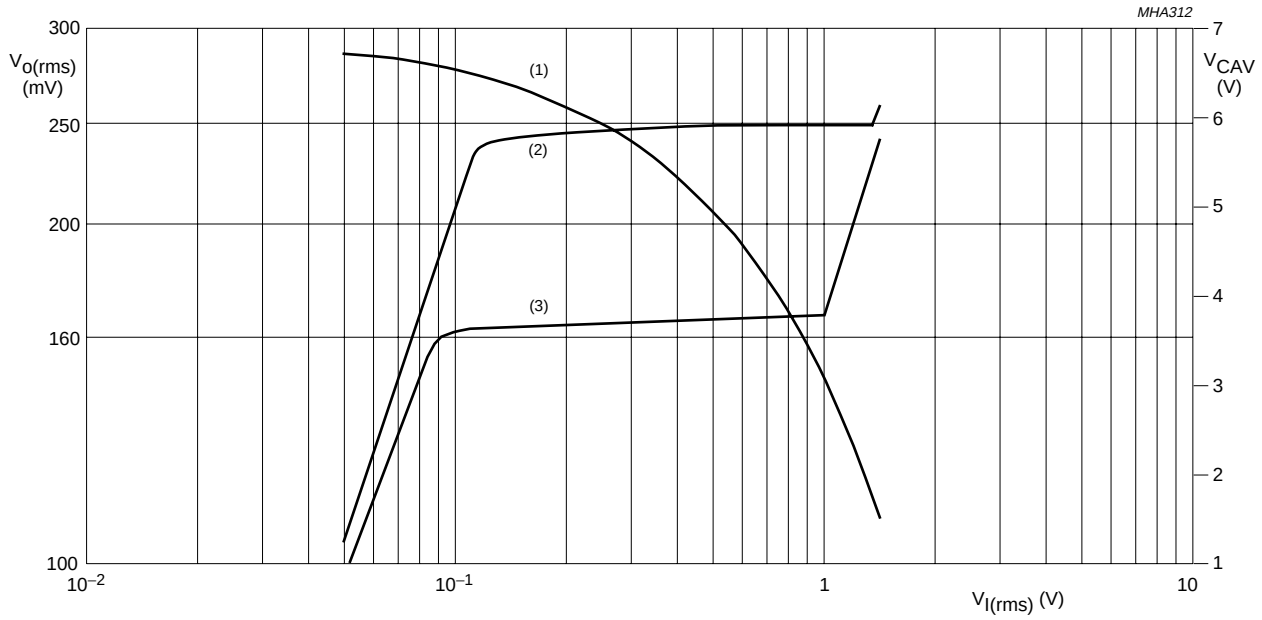


(1) see Table 23.
(2) see Table 23.
(3) see Table 23.

Fig.4 Pseudo (phase in degrees) as a function of frequency (left output).

Table 23 Explanation of curves in Fig.4

CURVE	CAPACITANCE AT PIN C_{PS1} (nF)	CAPACITANCE AT PIN C_{PS2} (nF)	EFFECT
1	15	15	normal
2	5.6	47	intensified
3	5.6	68	more intensified



(1) V_{CAV} AVL measured at pin EOL/EOR.

(2) $V_{o\ max(rms)}$ Y_1 axis output level in AVL operation with typically 200 mV.

(3) $V_{o\ min(rms)}$ Y_2 axis V_{CAV} DC voltage at pin C_{AV} corresponds with typical gain steps in range of +6 to −15 dB.

Fig.5 Automatic level control diagram.

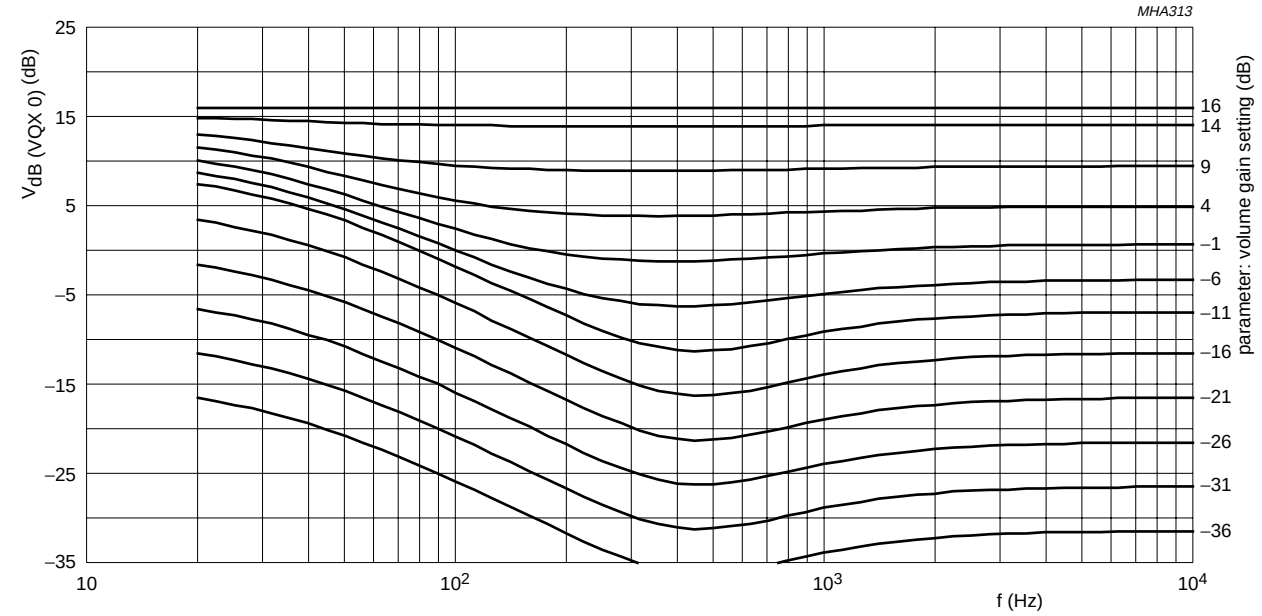


Fig.6 Volume control with loudness (including low roll-off frequency).

INTERNAL PIN CONFIGURATIONS

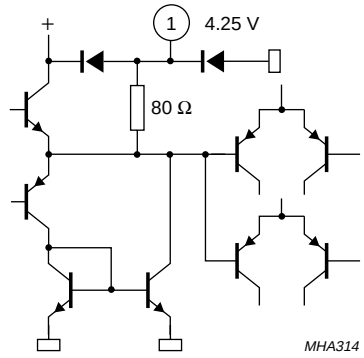


Fig.7 Pins OUTL, SOL, SOR and OUTR.

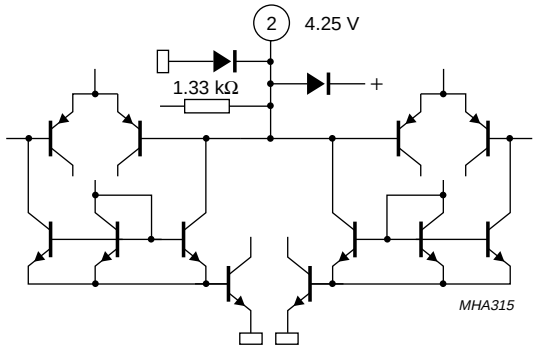


Fig.8 Pins LDL and LDR.

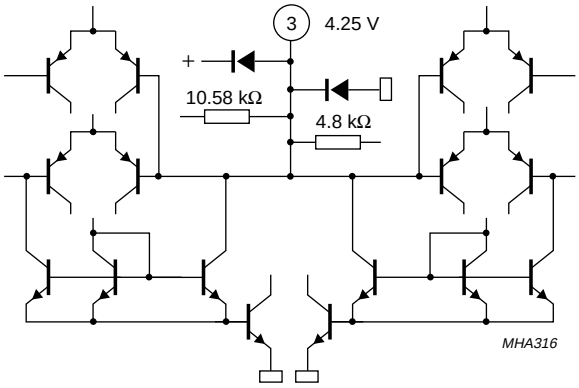


Fig.9 Pins VIL and VIR.

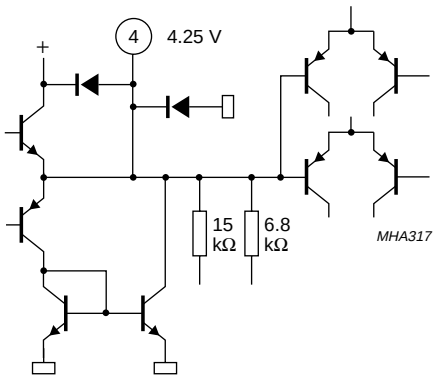


Fig.10 Pins EOL and EOR.

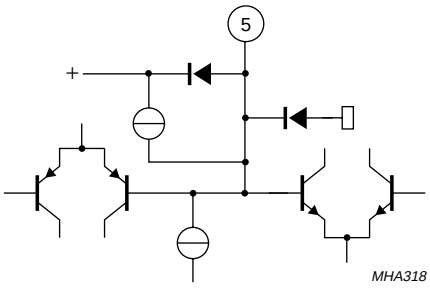


Fig.11 Pin C_{AV}.

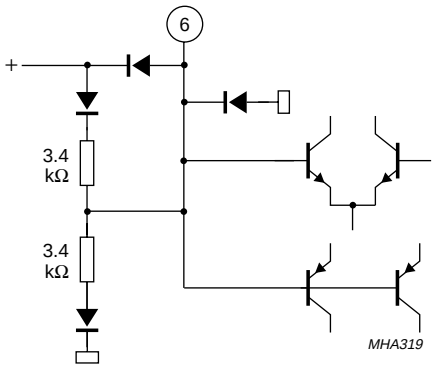


Fig.12 Pin V_{ref}.

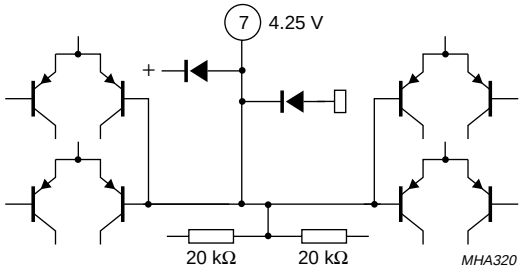


Fig.13 Pins LIL and LIR.

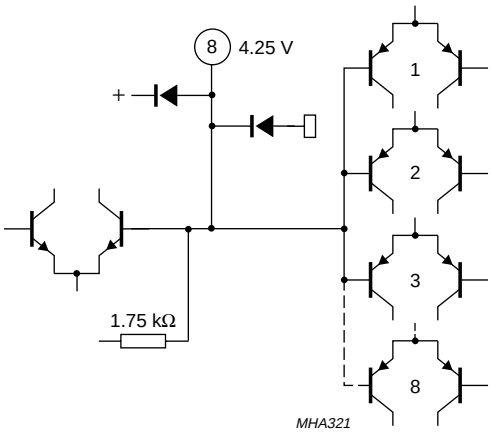


Fig.14 Pins AVL and AVR.

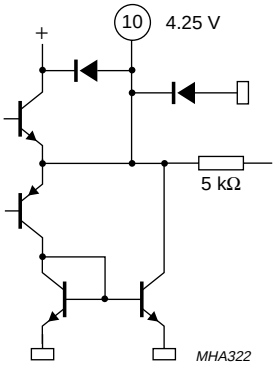


Fig.15 Pins LOL and LOR.

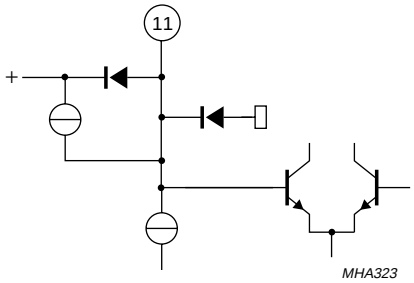


Fig.16 Pins C_{TW} and C_{TS}.

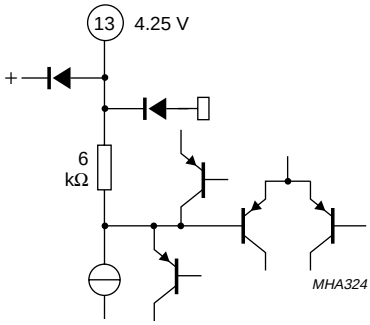


Fig.17 Pins C_W and C_S.

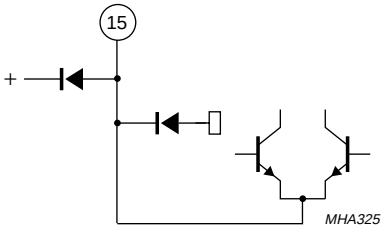


Fig.18 Pin VEO.

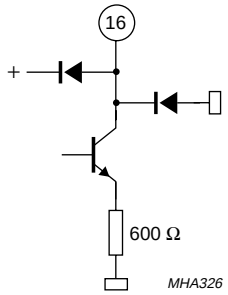


Fig.19 Pin VEI.

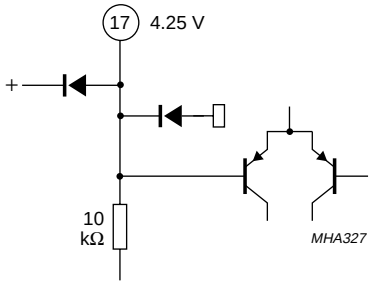


Fig.20 Pin C_{NR}.

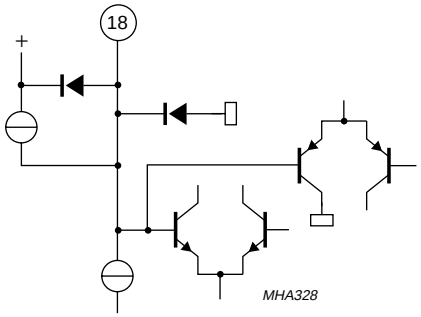


Fig.21 Pin C_M.

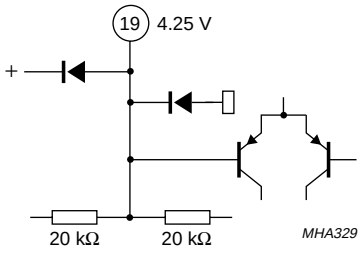


Fig.22 Pin C_{DEC}.

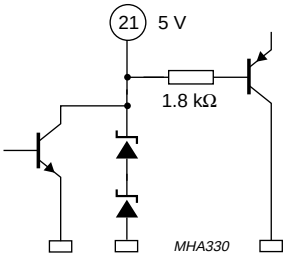


Fig.23 Pin SDA.

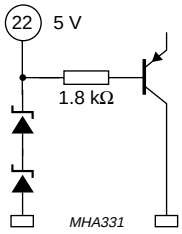


Fig.24 Pin SCL.

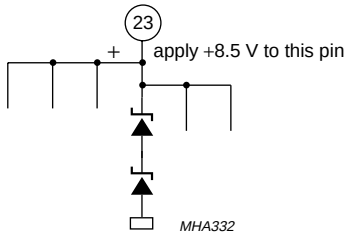


Fig.25 Pin V_{CC}.

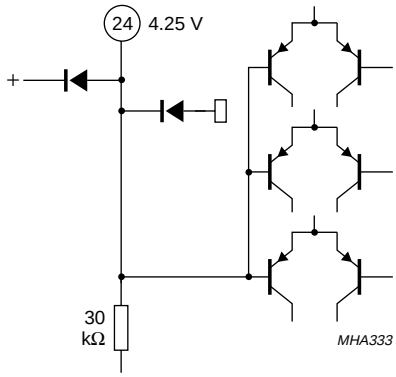


Fig.26 Pin COMP.

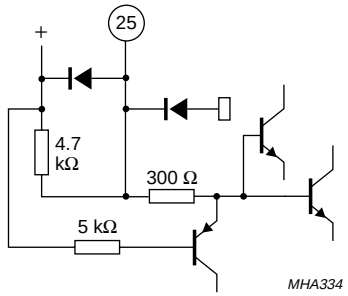


Fig.27 Pin V_{CAP}.

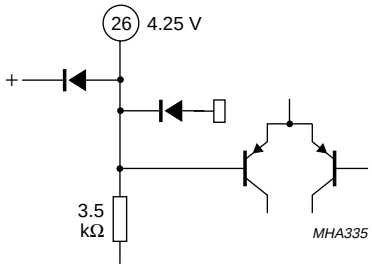


Fig.28 Pin C_{P1}.

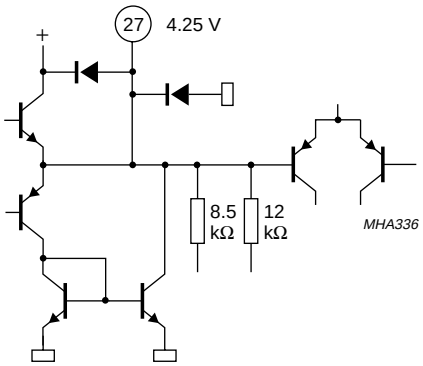


Fig.29 Pin C_{P2}.

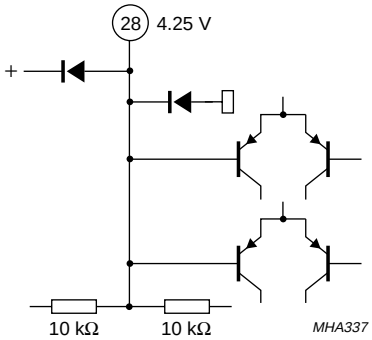


Fig.30 Pin C_{PH}.

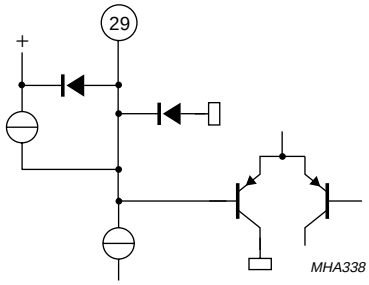


Fig.31 Pin C_{ADJ}.

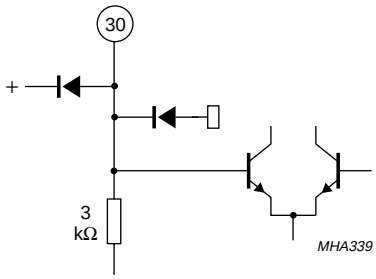


Fig.32 Pin CER.

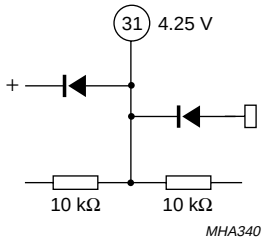


Fig.33 Pins C_{MO} and C_{SS}.

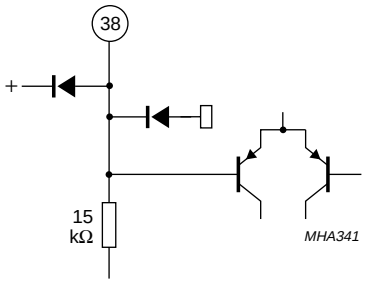
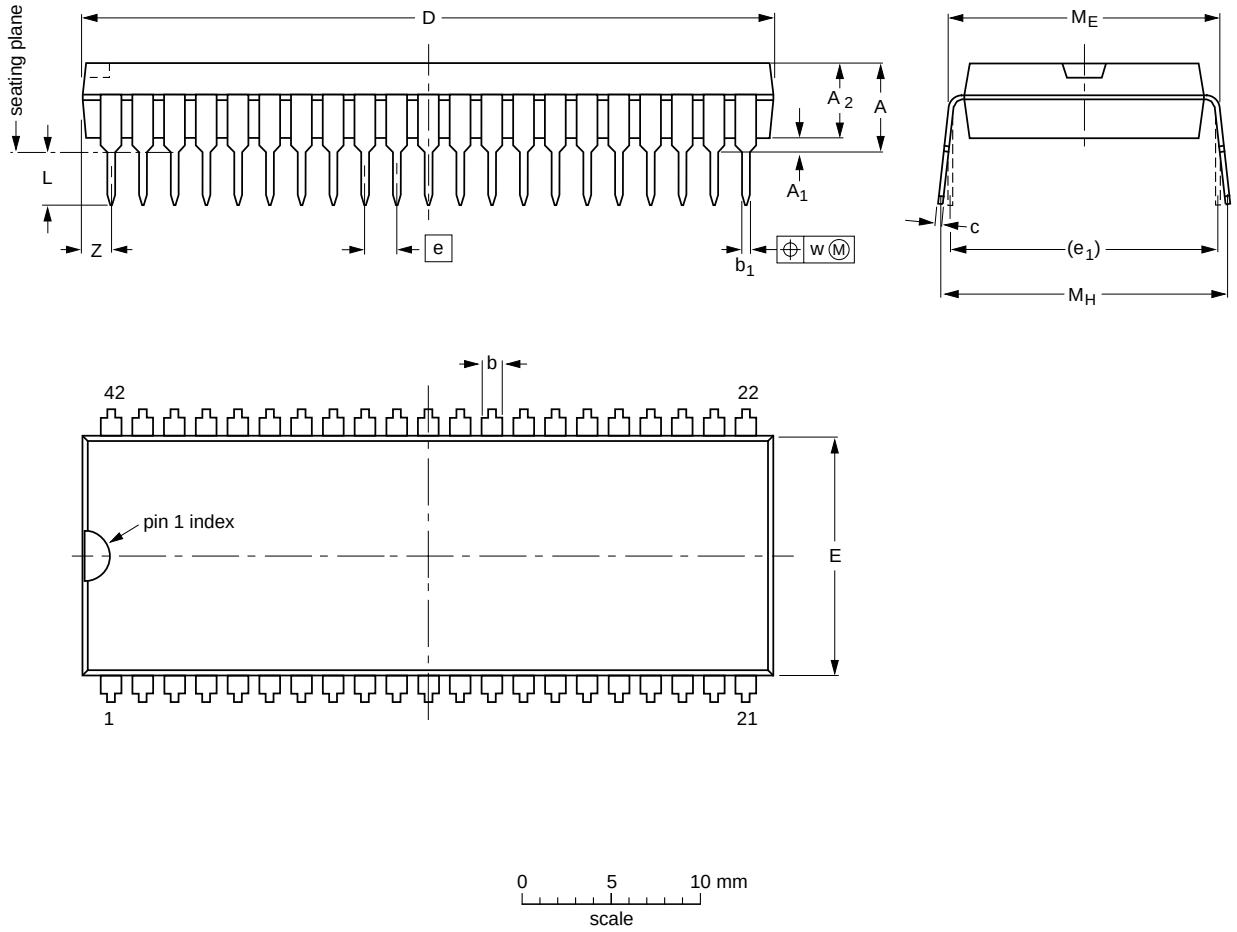


Fig.34 Pins C_{PS1} and C_{PS2}.

PACKAGE OUTLINES

SDIP42: plastic shrink dual in-line package; 42 leads (600 mil) **SOT270-1**



DIMENSIONS (mm are the original dimensions)

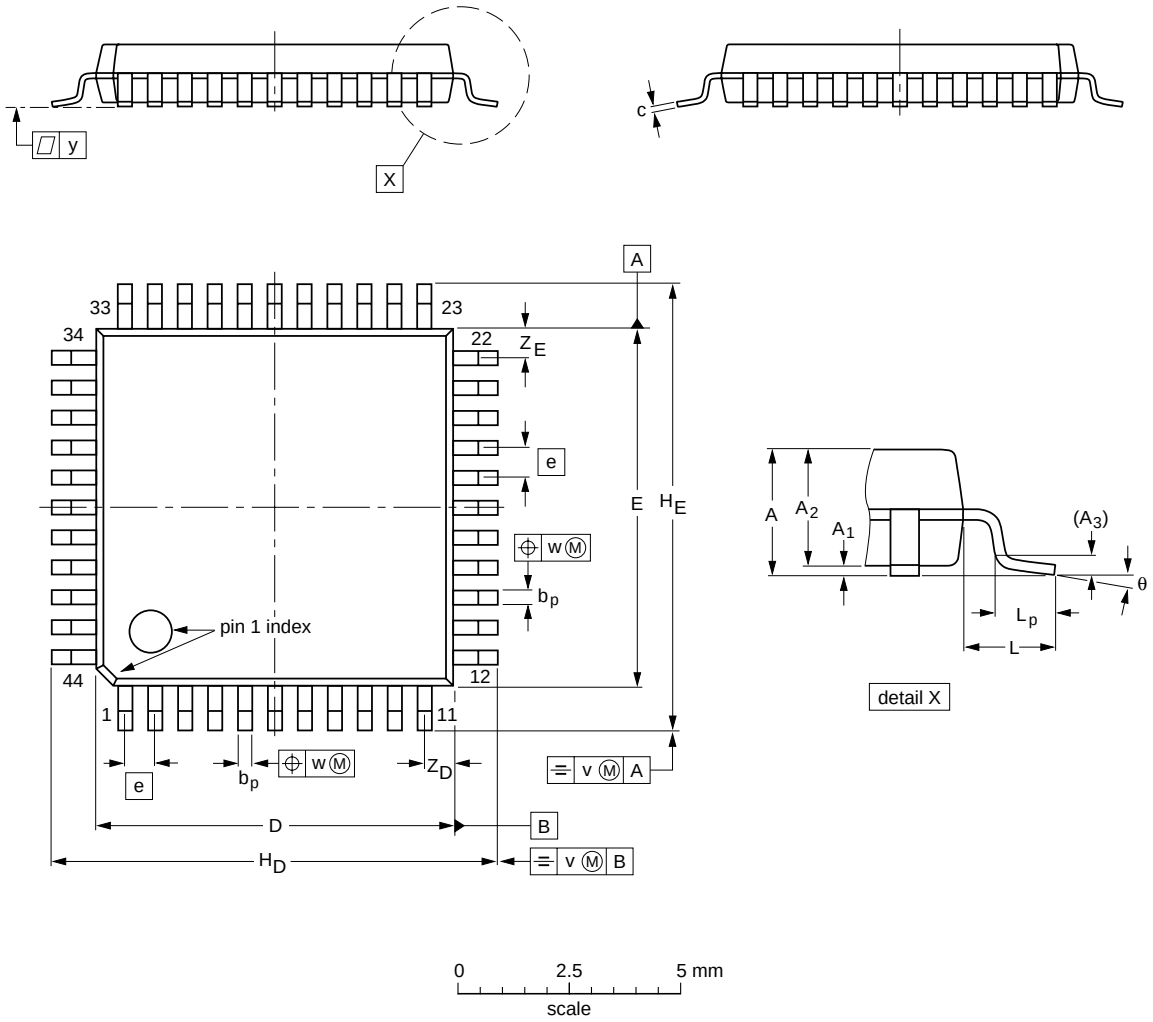
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	38.9 38.4	14.0 13.7	1.778	15.24	3.2 2.9	15.80 15.24	17.15 15.90	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT270-1						~~90-02-13~~ 95-02-04

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~95-02-04~~ 97-08-01

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

SDIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

QFP

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9398 510 63011).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary from 50 to 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheat for 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured. Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580/xxx

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,
Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2870, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

© Philips Electronics N.V. 1997 SCA53

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands 547047/1200/02/pp40 Date of release: 1997 Mar 11 Document order number: 9397 750 01766

Let's make things better.

Philips Semiconductors

PHILIPS